Architecting of TOPSTREAM™ WLAN
Heterogeneous Multi-Core for Wireless LAN

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Abstract In order to achieve IP phone capability in addition to conventional cell phone service, we need to realize a SoC for Wi-Fi, which requires about 3,000MIPS of computation power, with less than 100mW of power consumption. We applied TOPSTREAM™ Heterogeneous Multi-Core Platform and designed a SoC configuration for IEEE802.11 MAC and IEEE802.11b Base-Band processing, which is the TOPSTREAM™ WLAN. In order to reduce the energy consumed for data transfer on the internal busses and computations, singed magnitude expression is applied in both the matched filter implementation as well as on the 128-bit SIMD processor for I/Q signal processing. The TOPSTREAM™ WLAN realized Wi-Fi with 802.11b at 50MHz with four heterogeneous processors, and the power simulation result shown less than 100mW.

Keyword Multi-Core, Processor, SoC, Wireless LAN, SIMD

1. Introduction
IP phone capability via Wi-Fi network is expected as one of services for next generation cell phones. In order to achieve it, energy efficient implementation of SoC for IEEE802.11b is emerging. 802.11b was the first widely accepted wireless networking standard, followed by IEEE 802.11a and 802.11g. [1] The 802.11b operates in the ISM frequency band of 2.4GHz. The MAC function defines the procedure enables multiple stations to share a common medium for transmission and reception. The MAC layer uses the CSMA/CA technique to access the channel and avoids the collision between stations. The 802.11b has a maximum raw data rate of 11Mbit/s. Due to the CSMA/CA protocol overhead, in practice the maximum 802.11b throughput that an application can achieve is about 5.0Mbit/s over TCP and 7.1Mbit/s over UDP.

1.1. Wireless LAN System and Architecture
Cell phone provides modem function with base band processor, in addition we design a system to provide IP phone capability and internet access through Wireless LAN Processor and 2.4GHz RF device. The Wi-Fi Wireless LAN function is added on through a high speed serial I/O as shown in Figure 1. The Wireless LAN processor provides IEEE802.11 MAC and IEEE802.11b base band processing, and analog interface to the RF device.
The 802.11b is a direct extension of the Direct-Sequence Spread Spectrum (DSSS) modulation technique defined in the standard, and uses Complementary Code Keying (CCK) as its modulation technique, which is a variation on CDMA. The 802.11b is usually used in a point-to-multipoint configuration, wherein an access point communicates via an omni-directional antenna with one or more clients that are located in a coverage area around the access point. Typical indoor range is 30m at 11Mbit/s and 90m at 1Mbit/s.

Figure 1 Cell Phones with Wireless LAN

This paper describes on the platform based Multi-Core SoC architecture and design methodology for low-power Wireless LAN Processor. Performance and Power constraints are explain in Chapter 2, Architecture of TOPSTREAM™ WLAN is described in Chapter 3, which includes the instruction set architecture (ISA) and micro-architecture of Wireless LAN Processing Engine (WPE). In Chapter 4 introduces design techniques applied to the WPE for energy efficiency. Software Development Environment is described in Chapter 5. The evaluation results are shown in Chapter 6. We conclude this paper in Chapter 7.

2. Performance and Power Constraints

2.1. Performance requirements of Wireless LAN

We used ARM922T to study the computation load of the MAC layer, which includes Wired Equivalent Privacy (WEP) function. The test scenario assumes contention period with on Access Point(AP) and one STA in the network, and each transmitting data alternatively. With 1.5kByte of MSDU size and Channel utilization of 90%, at the highest data rate of 11Mbps, the MAC requires 4.71MIPS without WEP. The WEP requires 45.11MIPS at 11Mbit/s as shown in Error! Reference source not found.

We refer to the software based PHY implementation on TMS320C6416 8-way VLIW DSP that requires more than 1GHz of performance. 802.11b PHY requires computation load of 600MHz plus FPGA to implement. (Error! Reference source not found.)

The 802.11b uses Differential Binary Phase Shift Keying (DBPSK) for 1Mbit/s, Differential Quadrature Phase Shift Keying (DQPSK) for 2Mbit/s, and CCK (Complementary Code Keying). From the code analysis, we determine the most performance critical processing is receiving on the CCK, which is shown in Figure 2. [2][3][4] Channel Matched Filter (CMF) corrects incoming echoed signals arriving in multiple waves due to multi-path. The CMF is a short tap FIR, and once setup compute intensity is rather low.

Figure 2 Receiver functions on CCK(11Mbps)

The most time critical situation is a receiving preamble and detecting signal energy (ED), then control gain by AGC, synchronize to clock by Phase Rotor and adjust Tap of CMF during preamble. The time for preamble is 144us for long preamble and only 72us for short preamble as shown in Figure 3.

Figure 3 Frame structure and Preamble

3. Architecture of TOPSTREAM™ WLAN

3.1. Target Specifications

We defined the target specification as bellow

- Target : Low Power Wireless LAN
- Functionality : 802.11 MAC and 802.11b Base Band
  - Support WEP and WPA (Wi-Fi Protected Access)
  - Analog I/F with 2.4GHz RF device
  - High Speed Host I/F
- Performance : 3,000MIPS at 50MHz
- Power Consumption : less than 100mW

3.2. TOPSTREAM™ Platform

We utilized the TOPSTREAM™ Platform to design Multi-Core SoC for Wireless LAN Processor. The platform [5] is architected for the following features.

- Provide scalability up to 9 parallel processing cores.
- Provide a wide range of flexibility on DPE’s ISA
- Enable optimization of memory hierarchy
- Enable quick configuration and reuse for derivatives
It provides exploit of data-level, instruction-level, and task-level parallelism.

The Figure 4 depicts the organization of TOPSTREAM™ platform, which can scale from two processors consist of a MC and a DPE, and up to nine processor cores with a MC and eight DPEs as shown in the figure.

Each DPE may have difference ISA, but all DPEs share a 32-bit RISC ISA with minimum of a bank of 32-bit registers, which is sixteen registers. The basic ISA supports up to 16 register banks, 256 registers in total. In addition, each DPE can have additional ISA for application specific processing.

In addition to the CPS’s registers, the size of on-chip instruction memory (IM) and data memory (DM) can be configured for application tasks. Cache for MC is also configurable. These allows user to optimize memory hierarchy of target SoC for performance, cost, and energy-efficiency.

In order to provide scalability of processors and IP cores, TOPSTREAM™ bus is the heart of the TOPSTREAM™ platform. It consists of three shared busses with distributed arbitration logic. For instruction pre-fetch, each DPE accesses the IM through 128-bit I-bus. For data read and write, each DPE mainly accesses the DM through 128-bit D-bus, and each DPE also can access an external memory or on-chip I/Os through 128-bit S-bus. S-bus is also used by MC to preload instruction code into IM, to exchange data between external memory and DM, and to access on-chip I/Os.

There are essentially three steps to use TOPSTREAM™ platform.

1. Defining the Derivative architecture
2. Designing the Derivative DPE(s)
3. Integrating the Derivative SoC

Step (3) is very simple since there is no need to change the internal bus design. Following sections explain about step (1) and (2) in detail.

3.3. Architecting TOPSTREAM™ WLAN
First priority for architecting wireless processor for low power is to lower the operating frequency of processor for high compute intensive PHY layer. The target frequency of 50MHz is set based on estimation that a Multi-Core SoC consumes 2mW/MHz.

By taking the WLAN MAC and PHY algorithm written in C, we applied TOPSTREAM™ platform and optimized both processor’s architecture and wireless LAN software. The partitioning and algorithm of software are done in parallel with defining each processor’s ISA. It was bi-directional optimization between processor and software.

At first we split MAC into two, MAC without WEP and WEP/WPA. We partitioned PHY into three. PHY-I is the front-end from I/Q input through phase rotor, which is commonly used for all data rate. PHY-II is the signal processing for Fast Walsh Transform and Code Decision for receive. PHY-III is mainly for packet processing such as scramble and de-scramble as well as error correction. Since the PHY-I require less programmability than setting CMF FIR tap parameters and phase shift control, it is implemented in hardware.

![Figure 5 Approach for optimization](image)

We considered to provide scalability for future generation of Wireless LAN Applications, such as 802.11g, etc. Scalability to higher data rate Wireless LAN requires much more signal processing performance at PHY-II. The rest is rather linear increase on performance with increasing data rate. For energy-efficiency we considered to scale number of processors for future generation.

The Figure 6 shows the configuration of TOPSTREAM™ WLAN. Most compute intensive processor is WPE, which is 128-bit SIMD processor for wireless processing. The ISA of WPE support 8-bit, 16-bit, 32-bit packed integer as well as 8-bit, 16-bit packed
complex data which enables efficient computation on I/Q two dimensional vectored data expressed in Imaginary and Real in complex format.

**Figure 6  Organization of TOPSTREAM™ WLAN**

The RPE architecture is optimized for packet data processing such as scramble/de-scramble and CRC checking. For these computations, extensive operations on any bit field as well as bit field insertion and extraction are supported by RPE ISA.

For security, SPE support operations for random number generation and WEP/WPA encryption algorithms efficiently with 256Byte of local scratch pad memory.

The Table 1 summarizes the features of each unit on the TOPSTREAM™ WLAN configuration. In order

<table>
<thead>
<tr>
<th>Units</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC</td>
<td>Five Stage Pipelined 32-bit RISC processor</td>
</tr>
<tr>
<td>WPE</td>
<td>Five Stage Pipelined 128-bit SIMD processor</td>
</tr>
<tr>
<td>RPE</td>
<td>Five Stage Pipelined 32-bit RISC processor</td>
</tr>
<tr>
<td>SPE</td>
<td>Five Stage Pipelined 32-bit RISC processor</td>
</tr>
<tr>
<td>IM</td>
<td>Instruction Memory for DPEs : 32kByte</td>
</tr>
<tr>
<td>DM</td>
<td>Data Memory for DPEs : 32kByte</td>
</tr>
<tr>
<td>GE</td>
<td>Graphical Engine for LCD control</td>
</tr>
</tbody>
</table>

**3.4. ISA for WPE**

The WPE integrates 128-bit SIMD type PHY specific instructions in addition to a 32-bit RISC ISA. The 128-bit SIMD ISA supports for 8-bit, 16-bit, and 32-bit packed data in integer as well as in complex data format.

The ISA is based on 16-bit instruction length, and 16-bit prefixes are added for switch ISA between two, conditional execution, and register-bank switch. Since prefix decoder can be implemented to decode in parallel to the main decoder, usually there is no additional cycles are required for prefix.

WPE implements 54 instructions for 32-bit RISC, and 167 instructions for 128-bit SIMD including special 128-bit instructions.

On of effective SIMD instruction is FWT instruction, which is designed to accelerate Basic Fast Walsh Transform operations shown in Figure 7. 8 complex samples from \( x_0 \) through \( x_7 \) are represented in Real and Imaginary, and through FWT 64 complex correlations are taken, and right after FWT the biggest one is picked up from 64 complexes.

**Table 1  Features of TOPSTREAM™ WLAN**

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<td>Five Stage Pipelined 128-bit SIMD processor</td>
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<td>Five Stage Pipelined 32-bit RISC processor</td>
</tr>
<tr>
<td>SPE</td>
<td>Five Stage Pipelined 32-bit RISC processor</td>
</tr>
<tr>
<td>IM</td>
<td>Instruction Memory for DPEs : 32kByte</td>
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<td>DM</td>
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<tr>
<td>GE</td>
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</tbody>
</table>

**Table 2  Computation for FWT and Biggest Picker**

<table>
<thead>
<tr>
<th></th>
<th>Real Addition</th>
<th>Real Multiplication</th>
<th>Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>FWT</td>
<td>224</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Biggest Pick</td>
<td>64</td>
<td>128</td>
<td>63</td>
</tr>
</tbody>
</table>
### 3.5. Micro-Architecture of WPE

WPE is implemented with five pipeline stages, such as Instruction Fetch (IF), Instruction Decode (ID), Execution (EX), Memory Access (MA), and Write Back (WB).

There are following two features in the WPE micro-architecture:

1. Zero-Over-Head Loop
2. Parallel Processing of computation and Data Move

IF stage pre-fetches instruction code from Instruction Memory (IM), and stores the code into 32 byte of pre-fetch buffer. It also stores inner-loop code as a loop buffer. During a loop consists of less than 16 instructions, no branch stall nor instruction fetch happens.

MA can operate on load/store for both GRPs and DPRs in parallel to non-MA micro-instructions as shown in Figure 9.

This mechanism allows block data pre-load and post-store with no visible instruction execution cycles.

### 4. Design Techniques of WPE

#### 4.1. Design for Performance

There are three custom logics that are designed at RTL not only for increasing performance per hardware cost, but also for low power consumption to reduce gate size. Due to a lot of instruction in 64-bit SIMD operation, execution units becomes complex.

The most complex unit is MAU, which support multiply based 51 operations in byte or word, signed or unsigned, complement, and with saturation or without saturation. These operations include the FWT and PBBP64. In order to share hardware resources as much as possible, we constructed the MAU based on four 16-bit x 16-bit multipliers. Each 16-bit x 16-bit multiplier consists of four 8-bit x 8-bit multipliers and it supports both 16-bit and 8-bit multiply as well as summation of four 16-bit data. The 32-bit accumulator is attached for MAC operation and 32-bit saturation logic is following. For optimize speed and size of MAU, we applied 4:2 compressor based design for multipliers and accumulators.

### 5. Software Development Environment

In general, providing a room for software optimization is one of the key issues for Multi-Core SoC. The TOPSTREAM™ WLAN provides a high level of programmability for system control software with Intent embedded operating system with C/C++, Java compiler environment for MC. However, since the WPE and RPE works on very real time constraint environment within tight timing, we used the assembler to port the PHY software. The cycle budget for both PHY-II and PHY-III are 36 cycles at 50MHz, which are very limited steps to program. Figure 10 shows the cycle budget for PHY-I through PHY-III. Since PHY-I is operated at 22MHz, which is the same rate as AD converter sampling the I/Q signals, the cycle budget is only 16 cycles. Both WPE and RPE are running at 50MHz for PHY-II and PHY-III respectively, each processor has only 36 cycles. Although the TMS320C64 for PHY consumes 710 cycle for PHY-1 through PHY-III.
Figure 10 Cycle Budget for PHY Processing

In addition, as a scalable SoC design, we developed configurable ISS for TOPSTREAM™ WLAN for performance evaluation and functional verification of software ported and partitioned for TOPSTREAM™ WLAN. Table 4 summarizes the SDE.

Table 4 SDE of TOPSTREAM™ WLAN

<table>
<thead>
<tr>
<th></th>
<th>MC</th>
<th>WPE</th>
<th>RPE</th>
<th>SPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>C Compiler</td>
<td>✓</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>Assembler</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Monitor</td>
<td>✓</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>OS</td>
<td>✓</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>ISS (TS-ISIM)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HW/SW Co-Verif.</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

6. Evaluation Results

We designed the TOPSTREAM™ WLAN using RTL(VHDL) and burned into three Xilinx Vertex-II FPGAs as shown in Figure 11. The Evaluation Board runs at 25MHz.

Figure 11 TOPSTREAM™ WLAN Evaluation Board

For evaluating the Power Consumption, we synthesized RTL with the Design Compiler onto 0.18um TSMC technology with using the Low Power Library Power Compiler from Artisan. On chip SRAMs are all single port SRAM library from Artisan.

The total Gate size is 650kGate, and the power consumption at 50MHz is 93.6mW on Power Compiler.

WLAN RTL: VHDL 140,000 Lines
- MC: Master Controller
- WPE: Wireless Processor Engine
- RPE: RISC Processor Engine
- SPE: Security Processor Engine

Gates: 600KGates(Logic)+72KB(Cache)+256KB(Mem)
Process: TSMC 0.18u STD CMOS
- Library: Artisan Low Power Library
- Gate Density: 70KGates/mm2
- Power: 0.08uW/MHz/Gate

Chip Size: 44.08mm2 (Core:31.80mm2)
- Logic: 8.57 mm2 (600K/70K)
- Glue: 5.00 mm2 (ADC/DAC, SDIO)
- Cache: 3.83 mm2 (SRAM 72KB)
- Mem: 14.40mm2 (SRAM 32KB × 8=256KB)
- IO: 12.28 mm2

Speed: 50MHz
Power: ~100 mW

Figure 12 TOPSTREAM™ WLAN Parameters

7. Conclusions

The TOPSTREAM™ WLAN realizes a low power Multi-Core Wi-Fi SoC for Mobile Multimedia appliances. The WPE enhances energy-efficiency with the dedicated 128-bit ISA and energy aware implementation at higher level of design. The configuration with four heterogeneous processors, it consumes less than 100mW to perform 802.11 MAC and 802.11b PHY processing.

8. Reference